

AMENDMENTS TO THE CLAIMS

Claim 1 (Currently amended) A method for determining interface traps in a semiconductor/oxide interface of a MOS transistor comprising a bulk substrate, a source, a drain, a gate, and a silicon oxide layer beneath the gate, the method comprising:

grounding the bulk substrate, source, and drain;

applying a first gate pulse having a fixed low-level gate voltage (V_{gl}) and an increasing high-level gate voltage (V_{gh}) at a high gate pulse frequency on the gate so as to obtain a first charge-pumping ~~current (I_{CP})~~- V_{gh} -~~curve~~current I_{CP} - V_{gh} curve;

applying a second gate pulse having the same low-level gate voltage (V_{gl}) and the same increasing high-level gate voltage (V_{gh}) as the first gate pulse at a low gate pulse frequency on the gate so as to obtain a second I_{CP} - V_{gh} curve; and

subtracting the second I_{CP} - V_{gh} curve from the first I_{CP} - V_{gh} curve.

Claim 2 (Original) The method of claim 1 wherein the second I_{CP} - V_{gh} curve is approximately equal to a leakage current component.

Claim 3 (Original) The method of claim 1 wherein the silicon oxide layer has a thickness of less than 30 angstroms.

Claim 4 (Original) The method of claim 1 wherein the silicon oxide layer has a thickness that is in a direct tunneling regime.

Claim 5 (Original) The method of claim 1 wherein the high gate pulse frequency is about 1 MHz and the low gate pulse frequency is about 10^4 to 10^5 Hz.

Claim 6 (Currently amended) A method for testing a MOS transistor having an ultra-thin gate oxide layer, wherein the MOS transistor comprises a bulk substrate, a source, a drain, a gate, and an ultra-thin gate oxide layer disposed between the gate and the bulk substrate, the method comprising:

grounding the bulk substrate, source, and drain, wherein the source and the drain are electrically connected to each other;

5 applying a first gate pulse having a fixed low-level gate voltage (V_{gl}) and an increasing high-level gate voltage (V_{gh}) at a high gate pulse frequency on the gate so as to obtain a first I_{CP} - V_{gh} curve;

 applying a second gate pulse having the same low-level gate voltage (V_{gl}) and the same increasing high-level gate voltage (V_{gh}) as the first gate pulse at a low gate pulse frequency on the gate so as to obtain a second I_{CP} - V_{gh} curve; and

10 subtracting the second I_{CP} - V_{gh} curve from the first I_{CP} - V_{gh} curve so as to obtain a third I_{CP} - V_{gh} curve that is regarded as a real charge-pumping current curve at the low gate pulse frequency.

Claim 7 (Original) The method of claim 6 wherein the ultra-thin gate oxide layer has a thickness of less than 20 angstroms.

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Claim 8 (Original) The method of claim 6 wherein the ultra-thin gate oxide layer has a thickness that is in a direct tunneling regime.

AMENDMENTS TO THE DRAWINGS

The attached 10 pages of replacement sheets include changes to FIG. 1(c), FIGS. 3-7, and FIG. 9 and a newly submitted FIG. 10 presenting Table 1 originally presented in the specification. FIG. 1(a), FIG. 1(b), and FIG. 1(c) are now placed in separate sheets to replace the original sheet including FIG.1 (a), (b), and (c). In FIG.1(c), “windows” in the process block has been replaced with “window”. In FIGS. 3-7, and FIG. 9, “A” has been replaced with “Å”. In addition, 7 pages of annotated sheets showing changes made are also submitted.

Attachment:

10 Replacement Sheets; and

7 Annotated Sheets showing changes made in FIG. 1(c), FIGS. 3-7, and FIG. 9.